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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,847	07/10/2003	Chad Allen Adams	AUS920030370US1	1736

7590 07/13/2004

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,847	ADAMS ET AL.	
	Examiner	Art Unit	
	Pho M Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-18* is/are allowed.

6)☒ Claim(s) *1,3-7,9-13,19 and 20* is/are rejected.

7)☒ Claim(s) *2 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because it uses the phrase "the present invention" in line 2, which is implied. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claim 1 is objected to because of the following informalities:

In claim 1, line 13: Please insert --and-- after "semicolon".

In claim 9, line 8: Please replace "bit_line ;" with --bit_line;--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-7, 9-13, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Christensen et al. (US. 6,741,493).

Regarding claim 1, Christensen et al. in Fig. 1 discloses a SRAM cell (SRAM cell 1) having a true node and a complement node comprising a continuous bit-line (CBLC 1) coupled to the complement node of the SRAM cell (1);

a true local bit-line (LBLT 1) coupled to the true node of the SRAM cell (SRAM cell1);

a first (108) and second (110) positive field effect transistor;

a pre-charge line (pre-charge circuit 120 include transistor 126 with a gate coupled to a pre-charge signal, a source coupled to Vdd and a drain coupled to the LBLT 1) coupled to the gate of the first (108) positive field effect transistor (word-line

102 coupled to gate input positive field effect transistor 108 and LBLT 1 coupled to positive field effect transistor 108);

a write true bit-line (LBLT 1) coupled to the gate of the second (110) positive field effect transistor (word-line 102 coupled to gate input positive field effect transistor 110 and LBLT 1 coupled to positive field effect transistor); and

a negative field effect transistor (128) coupled to the write true bit-line (LBLT 1) through the gate of the negative field effect transistor (write circuit 122 include an negative field effect transistor 128 with a drain coupled to the LBLT 1, a gate coupled to the output of 124 circuit and a source coupled to ground).

With respected to claim 3, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the SRAM cell (SRAM cell 1) that the continuous bit-line (CBLC 1) is coupled to an output of a NAND (132) gate.

With respected to claim 4, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the SRAM cell (SRAM cell 1) that a write enable input (WRITE ENABLE complement) coupled to an input of the NAND gate (NAND gate 132 is coupled to the inverter 134 to receive a write enable signal).

With respected to claim 5, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the SRAM cell (SRAM cell 1) that the data input (DATA IN 1) coupled to an input of the NAND gate (NAND gate 132 is coupled to the inverter 134 to receive a write enable signal and receives the data input DATA IN 1).

With respected to claim 6, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the SRAM cell (SRAM cell 1) that an output of a NOR (130) gate coupled to the write true bit-line (the output of NOR gate 130 coupled to gate transistor 128 with a drain coupled to the true bit-line LBLT 1).

With respected to claim 7, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the SRAM cell (SRAM cell 1) that the source of the negative field effect transistor (128) is coupled to electrical ground (the source of the transistor 128 terminal coupled to ground).

Regarding claim 9, Christensen et al. in Fig. 1 discloses a method of reading indicia from an SRAM cell (SRAM cell 1) comprising

generating a low value (when the write enable (WRITE ENABLE) signal is high, the NOR gate 130 output an inverted signal of data input (DATA IN 1) onto the write (LOCAL WRITE LINE), the NAND gate 132 output an inverted signal of the data input onto the continuous bit-line (CBLC 1) which is adjust the signal value on the local true bit-line (LBLT 1)) on a write true line (see column 3, lines 41-49);

generating a high value (when the write enable (WRITE ENABLE) signal is low, the NOR gate 130 output a low local write signal (DATRA IN 1), the NAND gate 132 output a high signal onto the continuous bit-line (CBLC1)) on a continuous bit-line (see column 3, lines 35-40) and evaluating the true node of the SRAM cell (SRAM cell 1).

With respected to claim 10, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the method comprising transition a word-line (102) value

from a low value (when the write enable (WRITE ENABLE) signal is high, the NOR gate 130 output an inverted signal of data input (DATA IN 1) onto the write (LOCAL WRITE LINE), the NAND gate 132 output an inverted signal of the data input onto the continuous bit-line (CBLC 1) which is adjust the signal value on the local true bit-line (LBLT 1)) to a high value (when the write enable (WRITE ENABLE) signal is low, the NOR gate 130 output a low local write signal (DATRA IN 1), the NAND gate 132 output a high signal onto the continuous bit-line (CBLC1)).

With respected to claim 11, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the method comprising conveying indicia from the true node of the SRAM cell (SRAM cell 1) to a global bit-line (LBLT 1).

With respected to claim 12, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the method comprising a step of inputting a high value (when the write enable (WRITE ENABLE) signal is low, the NOR gate 130 output a low local write signal (DATRA IN 1), the NAND gate 132 output a high signal onto the continuous bit-line (CBLC1)) into a write enable line (WRITE ENBLE).

With respected to claim 13, Christensen et al. disclose, in Fig. 1 and respective portion of the specification, the method comprising inverting a signal (write enable signal is high, the NOR 130 output an inverted signal of the data input (DATA IN 1) onto the CBLC 1) from the write enable line (WRITE ENABLE) (see column 3, lines 41-45).

Regarding claim 19, Christensen et al. in Fig. 1 discloses a computer program product for reading indicia from an SRAM cell, the computer program having a medium with a computer program comprising:

computer code for generating a low value (when the write enable (WRITE ENABLE) signal is high, the NOR gate 130 output an inverted signal of data input (DATA IN 1) onto the write (LOCAL WRITE LINE), the NAND gate 132 output an inverted signal of the data input onto the continuous bit-line (CBLC 1) which is adjust the signal value on the local true bit-line (LBLT 1)) on a write true line (see column 3, lines 41-49);

computer code for generating a high value (when the write enable (WRITE ENABLE) signal is low, the NOR gate 130 output a low local write signal (DATRA IN 1), the NAND gate 132 output a high signal onto the continuous bit-line (CBLC1)) on a continuous bit-line (see column 3, lines 35-40) and evaluating the true node of the SRAM cell (SRAM cell 1).

Regarding claim 20, Christensen et al. in Fig. 1 discloses a processor for reading indicia from an SRAM cell, the processor including a computer program comprising:

computer code for generating a low value (when the write enable (WRITE ENABLE) signal is high, the NOR gate 130 output an inverted signal of data input (DATA IN 1) onto the write (LOCAL WRITE LINE), the NAND gate 132 output an inverted signal of the data input onto the continuous bit-line (CBLC 1) which is adjust

the signal value on the local true bit-line (LBLT 1)) on a write true line (see column 3, lines 41-49);

computer code for generating a high value (when the write enable (WRITE ENABLE) signal is low, the NOR gate 130 output a low local write signal (DATRA IN 1), the NAND gate 132 output a high signal onto the continuous bit-line (CBLC1)) on a continuous bit-line (see column 3, lines 35-40) and evaluating the true node of the SRAM cell (SRAM cell 1).

Allowable Subject Matter

6. Claims 2 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, the prior art of record do not disclose or suggest the drain of the negative field effect transistor is coupled to the source of the second positive field effect transistor.

Regarding claim 8, the prior art of record do not disclose or suggest the local true bit-line is coupled to the source of the first positive field effect transistor.

8. Claims 14-18 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "generating a complementary continuous bit-line signal, driving the true node of the SRAM high if the write true signal is low and driving the true node of the SRAM low if the write true signal is high" as claimed in the independent claim 14.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schneider (US. 6,108,256) disclosed the pre-charge circuit includes a set of pre-charge transistors is coupled to the bit lines.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see

http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
09 July 2004

Pho M. Luu
Patent Examiner
Art Unit 2824